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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,105	11/17/2003	Leonard Forbes	1303.011US2	3271

21186 7590 05/16/2005

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,105	FORBES, LEONARD	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-62 and 72-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *46-62* is/are allowed.

6)☒ Claim(s) *72-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Preliminary Amendment

1. Acknowledgment is made of applicant's Preliminary Amendment, filed 17 November 2003. The changes and remarks disclosed therein were considered.

Claims 1-45 and 63-71 have been cancelled. Therefore, claims 46-62 and 72-76 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 17 November 2003. The information disclosed therein was considered.

Specification

3. Claims 72 and 74-76 are objected to because of the following informalities:

Claim 72, in the last line, recites "a selected current line" which appears to be an error. It will be understood as --a selected column line--.

Claims 74 and 76 depend on claim 71 which is cancelled. It will be understood to depend on claim 73.

Claim 75 recites "the PMOS transistor" and "the NMOS transistor" which appear to lack antecedent bases. This claim will be understood to depend on claim 73.

Appropriate correction is required.

4. The disclosure is objected to because of the following informalities:

In the first paragraph of the specification, the status of the parent application should be updated; namely, the parent application has matured into U.S. Patent No. 6,654,275.

Appropriate correction is required.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 72-76 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 36, 39 and 51-54 of U.S. Patent No. 6,654,275. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claim 72 of the instant application, claims 36 and 39 of Patent recite a SRAM circuit, comprising: a memory array, a controller, a row line voltage generator, a column line voltage generator, and a column line current detector (see claim 39 of Patent); coupling the controller to the row line voltage generator, the column line voltage generator, and the column

line current detector; coupling the row line voltage generator to row lines within the memory array such that the controller is able to vary a potential on a selected row line (or selectively adjusting a row potential, in claim 36 of Patent); coupling the column line voltage generator to column lines within the memory array such that the controller is able to vary a potential on one or more selected column lines (or, selectively adjusting a column potential, in claim 36 of Patent); and coupling the column line current detector to the column lines within the memory array such that the controller is able to determine current flow on a selected column line (see claim 39 of Patent).

The Patent claims do not recite a method of forming the above SRAM circuit with steps of providing and coupling the recited elements. However, since the SRAM circuit recited in said Patent claims is a product of a directly related process or method recited in the claims of the instant application, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to form the above SRAM circuit by providing and coupling the recited elements (as recited in the application claims) using fabrication or manufacturing processes well known in the art.

Regarding claims 73-76, claims 36 and 39 disclose a method as above, with the exception of the first transistor and the second transistor being PMOS and NMOS transistors, as recited in claims 73-76 of the instant application.

Claims 51-54 of Patent recite providing a memory array including providing a plurality of memory cells (inherent in a memory system of claim 51 of Patent), each cell being provided by: forming a PMOS transistor with a gate; forming an NMOS transistor with a gate; coupling

the PMOS transistor gate in series with the NMOS transistor; and coupling the NMOS transistor gate in series with the PMOS transistor (see claim 51 of Patent); forming a memory cell by forming a PMOS transistor with a gate and forming an NMOS transistor with a gate includes forming a lightly doped polysilicon gate for both the PMOS transistor and the NMOS transistor (claim 52 of Patent); coupling the PMOS transistor and the NMOS transistor gate between a PWRP power supply and a first reference line; and coupling the NMOS transistor and the PMOS transistor gate between a PWRN power supply and a second reference line (claim 53 of Patent); coupling the PMOS transistor and the NMOS transistor gate between a constant power supply and a ground reference line; and coupling the NMOS transistor and the PMOS transistor gate between a column line with an adjustable potential and a row line with an adjustable potential (claim 54 of Patent).

Since claim 51 of Patent recites coupling the PMOS transistor gate in series with the NMOS transistor, and coupling the NMOS transistor gate in series with the PMOS transistor, which essentially forms a same structure as that recited in claim 36 of Patent, one of ordinary skill in the art would use PMOS and NMOS transistors (as recited in claims 51-54 of Patent) as the first and second transistors of claims 36 and 39 of Patent, for the purpose of providing a specific details of the transistors for the operation of the SRAM circuit.

Allowable Subject Matter

7. Claims 46-62 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 46, 50 and 56, the prior arts of record do not disclose or suggest a method as recited in claim 46, 50 or 56, and particularly, increasing Vdiff by an increment less than a transistor threshold voltage and determining whether the increased Vdiff results in a current flow on the column line of the selected memory cell, or increasing Vdiff by an increment more than a transistor threshold voltage to set the selected memory cell to a one state (i.e., a transistor threshold voltage provides the basis for the amount of Vdiff increment either to read or write to a cell).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

ANH PHUNG
PRIMARY EXAMINER